Claims

We claim:

1. An electronic structure, comprising:

a substrate layer that includes a first electronic device;

a first insulative layer on the substrate layer;

a first damascene conductive wire/stud having a lower portion in the first insulative layer and an upper portion above the first insulative layer;

a subtractive etch metallic cap on the upper portion of the first damascene conductive wire/stud and in conductive contact with the first damascene conductive wire/stud;

a second insulative layer on the first insulative layer, wherein the second insulative layer covers the subtractive etch metallic cap; and

a damascene conductive wiring line structure within the second insulative layer such that the damascene conductive wiring line structure is above the subtractive etch metallic cap and is conductively coupled to the subtractive etch metallic cap.

2. The electronic structure of claim 1, wherein the lower portion of the first damascene conductive wire/stud is conductively coupled to a first portion of the first electronic device.

3. The electronic structure of claim 2, further comprising a second damascene conductive wire/stud having a lower portion in the first insulative layer and an upper portion above the first insulative layer, wherein the lower portion of the second damascene conductive wire/stud is

conductively coupled to a second portion of the first electronic device, and wherein the subtractive etch metallic cap is in conductive contact with the second damascene conductive wire/stud.

4. The electronic structure of claim 3, wherein the first electronic device is a field effect transistor (FET), wherein the first portion of the first electronic device includes a gate of the FET, and wherein the second portion of the first electronic device is selected from the group consisting of a source of the FET and a drain of the FET.

5. The electronic structure of claim 2, wherein the first electronic device is selected from the group consisting of an MOS capacitor, a resistor, an inductor, a charged coupled device, and a light emitting diode.

6. The electronic structure of claim 2, wherein the substrate layer further comprises a second electronic device, and wherein the electronic structure further comprises:

a second damascene conductive wire/stud having a lower portion in the first insulative layer and an upper portion above the first insulative layer, wherein the lower portion of the second damascene conductive wire/stud is conductively coupled to the second electronic device; and

a damascene conductive wiring line within the second insulative layer, wherein the damascene conductive wiring line is above the second damascene conductive wire/stud and is insulatively isolated from the second damascene conductive wire/stud.

7. The electronic structure of claim 6, further comprising a second subtractive etch metallic cap on the upper portion of the second damascene conductive wire/stud and in conductive contact with the second damascene conductive wire/stud.

8.The electronic structure of claim 1, wherein the substrate includes a shallow trench isolation (STI), and wherein the lower portion of the first damascene conductive wire/stud is on the STI.

9. The electronic structure of claim 1, further comprising:

a second subtractive etch metallic cap on the first insulative layer; and

a dual damascene within the second insulative layer such that the dual damascene is above the second subtractive etch metallic cap and is conductively coupled to the second subtractive etch metallic cap.

10. The electronic structure of claim 1, wherein the subtractive etch metallic cap has a thickness between about 50 nm and about 300 nm.

11. The electronic structure of claim 1, wherein the subtractive etch metallic cap includes an electrically conductive material selected from the group consisting of tungsten, tantalum, titanium nitride, aluminum with copper doping, tantalum nitride, tungsten nitride, gold, silver, platinum, copper, palladium, and combinations thereof.

12. The electronic structure of claim 1, wherein the first damascene conductive wire/stud includes an internal seam or void oriented lengthwise within the first damascene conductive

wire/stud.

13. The electronic structure of claim 1, wherein the subtractive etch metallic cap includes a first electrically conductive material, and wherein the first damascene conductive wire/stud includes a second electrically conductive material which differs from the first electrically conductive material.

14.The electronic structure of claim 13, wherein the first electrically conductive material is selected from the group consisting of tungsten, tantalum, titanium nitride, aluminum with copper doping, tantalum nitride, tungsten nitride, gold, silver, platinum, copper, palladium, alloys thereof, and combinations thereof, and wherein the second electrically conductive material is selected from the group consisting of polysilicon, tungsten, aluminum, copper, tantalum, and titanium nitride, alloys thereof, and combinations thereof.

15. An method for forming an electronic structure, comprising the steps of:

providing a substrate layer that includes a first electronic device;

forming a first insulative layer on the substrate layer;

forming a first damascene conductive wire/stud in the first insulative layer;

removing a top portion of the first insulative layer such that an upper portion of the first damascene conductive wire/stud is above the first insulative layer after said removing;

forming a metallic capping layer on the first insulative layer such that the metallic capping layer is in conductive contact with the first damascene conductive wire/stud;

subtractively etching a portion of the metallic capping layer to form a subtractive etch metallic cap on the upper portion of the first damascene conductive wire/stud such that the subtractive etch metallic cap is in conductive contact with the first damascene conductive wire/stud;

forming a second insulative layer on the first insulative layer, wherein the second insulative layer covers the subtractive etch metallic cap; and

forming a damascene conductive wiring line structure within the second insulative layer such that the damascene conductive wiring line structure is above the subtractive etch metallic cap and conductively coupled to the subtractive etch metallic cap.

16. The method of claim 15, wherein the step of forming a first damascene conductive wire/stud includes conductively coupling a lower portion of the first damascene conductive wire/stud to a first portion of the first electronic device.

17. The method of claim 16, further comprising forming a second damascene conductive wire/stud in the first insulative layer such that a lower portion of the second damascene conductive wire/stud is conductively coupled to a second portion of the first electronic device,

wherein the removing step results in an upper portion of the second damascene conductive wire/stud being above the first insulative layer,

wherein the step of forming a metallic capping layer results in the metallic capping layer being in conductive contact with the second damascene conductive wire/stud, and

wherein the subtractively etching step results in the subtractive etch metallic cap being in conductive contact with the second damascene conductive wire/stud.

18. The method of claim 17, wherein the first electronic device is a field effect transistor (FET), wherein the first portion of the first electronic device includes a gate of the FET, and wherein the second portion of the first electronic device is selected from the group consisting of a source of the FET and a drain of the FET.

19. The method of claim 16, wherein the first electronic device is selected from the group consisting of an MOS capacitor, a resistor, an inductor, a charged coupled device, and a light emitting diode.

20. The method of claim 16, wherein the substrate layer further comprises a second electronic device, and wherein forming the electronic structure further comprises:

forming a second damascene conductive wire/stud in the first insulative layer such that a lower portion of the second damascene conductive wire/stud is conductively coupled to a portion

of the second electronic device, wherein the removing step results in an upper portion of the second damascene conductive wire/stud being above the first insulative layer, and wherein the step of forming a metallic capping layer results in the metallic capping layer being in conductive contact with the second damascene conductive wire/stud; and

forming a damascene conductive wiring line within the second insulative layer, wherein the damascene conductive wiring line is above the second damascene conductive wire/stud and is insulatively isolated from the second damascene conductive wire/stud.

21. The method of claim 20, wherein the subtractively etching step etches away all conductive material of the metallic capping layer that had been in conductive contact with the second damascene conductive wire/stud.

22. The method of claim 15, wherein the substrate includes a shallow trench isolation (STI), and wherein the step of forming a first damascene conductive wire/stud includes forming a lower portion of the first damascene conductive wire/stud on the STI.

23. The method of claim 15, wherein the subtractively etching step further comprises forming a second subtractive etch metallic cap on the first insulative layer such that the second subtractive etch metallic cap is insulatively isolated, and further comprising forming a dual damascene within the second insulative layer such that the dual damascene is above the second subtractive etch metallic cap and is conductively coupled to the second subtractive etch metallic cap.

24. The method of claim 15, wherein the metallic capping layer has a thickness between about 50 nm and about 300 nm.

25. The method of claim 15, wherein the metallic capping layer includes an electrically conductive material selected from the group consisting of tungsten, tantalum, titanium nitride, aluminum with copper doping, tantalum nitride, tungsten nitride, gold, silver, platinum, copper, palladium, and combinations thereof.

26. The method of claim 15, wherein the first damascene conductive wire/stud includes an internal seam or void oriented lengthwise within the first damascene conductive wire/stud.

27. The method of claim 15, wherein the subtractively etching step includes selective etching of the portion of the metallic capping layer with respect to the first damascene conductive wire/stud, wherein the metallic capping layer includes a first electrically conductive material, and wherein the first damascene conductive wire/stud includes a second electrically conductive material which differs from the first electrically conductive material.

28. The method of claim 27, wherein the first electrically conductive material is selected from the group consisting of tungsten, tantalum, titanium nitride, aluminum with copper doping, tantalum nitride, tungsten nitride, gold, silver, platinum, copper, palladium, alloys thereof, and combinations thereof, and wherein the second electrically conductive material is selected from the group consisting of polysilicon, tungsten, aluminum, copper, tantalum, and titanium nitride, alloys thereof, and combinations thereof.